DVCon Japan 2024 Program Time Table

Time	Hall A General	Conf E Tech Track 1	Conf F Tech Track 2	Conf G Tech Track 3	Conf H Tech Track 4	Hall I Exhibition
8:20 - 8:50	Registration					
	General Sessions					
8:50 - 9:00	Opening Speech					
9:00 - 9:30	Accellera Updates Accellera Chair - Lu Dai					
9:30 - 10:30	Keynote Yasuhiko Ohta, Nikkei Shinbun Semiconductors change the world --From the national security and geopolitical perspective					
	Tutorial Sessions					
10:30 - 11:20	Cadence Is AI the “magic bullet” for solving the growing IP and SoC verification challenges ?	Accellera CDC Working Group Hierarchical CDC and RDC closure with standard abstract models				
11:20 - 11:40	Break for Lunch					Break for Lunch
	Luncheon Session					
11:40 - 12:30	Siemens EDA Verification methodologies for high-level synthesis, considering the contrast between RTL design and high-level design					
		Technical Sessions - Paper Presentation				
12:30 - 13:00		Quality Driven Analysis of Clock Tree Network using "Accelerated Clock Reference Model Generator"	Solving Memory Configurations Challenge with SV-Rand Verification Flow	Exploring Software-Defined Vehicles through Digital Twin Simulation with Extensible Prototyping FPGA: A Tool Perspective	Conquering UCIe 1.1 Multi-die System Verification Challenges	
13:00 - 13:30		Data integrity checker for Coherency Verification	Having Your Cake and Eating It Too - Programming UVM Sequences with DPI-C	Profiling and Optimization of Level 4 vECU Performance for faster ISO26262 Testing	[Short] Ensuring DRAM Compliance: Novel Verification Techniques for Refresh and Refresh Management in Modern Dram Architecture [Short] Enhancing PHY Design Verification: A Tailored VIP Solution for PIPE Interface-Based Designs	
13:30 - 14:00		Hardware/Software co-design and co-verification of embedded systems	Maximizing Verification Productivity Using UVM and Dynamic Test Loading	New Serial NAND Flash Octal DDR Feature, Its Verification Challenges and Solution for the Automotive Application Space	Veryl: A New Hardware Description Language as an Alternative to SystemVerilog	Exhibition
14:00 - 14:30		Break				
		Technical Sessions - Paper Presentation				
14:30 - 15:00		Quantization Methodology based on Value Range Analysis	Noise Reduction in Coverage-Based Formal Verification	Optimizing UPF Integration Efficiency through Enabling Automation with UPVM for Unified Power Verification		
15:00 - 15:30		Impact of a 64-bit Vedic Multiplier on Processor, Multi-Core, and DSP Performance	Introduction of CHERI and how it works	Uncore Emulation - Performance Validation with Synthesizable Traffic Generators		
15:30 - 16:00		Break				
		Tutorial Sessions				
16:00 - 16:50		Steering Committee Portable Stimulus Standard Update	Siemens EDA Introducing Smart Verification Unleashing the Potential of AI Within Functional Verification	Steering Committee A Practical Guide to SA-EDI Methodology		
16:50 - 17:40		Art-Graphics A Subjective Review on IEEE Std 1800-2023	Synopsys Low Power Verification Using Formal Technology	Codasip GmbH The way we walk around RISC-V		
17:40 - 20:30						Networking & Best Paper Award Ceremony